REMARKS

The Examiner's action of March 26, 2009 is noted in which the claims are variously rejected under 35USC112 and 35USC102.

Applicants have amended Claim 1 to recite that what is claimed is an interconnect fabric, thus eliminating the 35USC112 second paragraph rejection of the claims. Applicants have also amended Claim 14 to recite "the interconnect fabric of Claim 1". Applicants therefore request removal of this ground of rejection.

This leaves the rejection of the claims under 35USC102 in view of the Marshall et al. reference

Applicants have revised Claim 1 to positively recite that the reconfigurable interconnect layer provides a switching function to set the connections for the physical layer, see Specification, Page 7, Line 6.

Nowhere is this shown or taught in the Marshall et al. reference

First, nowhere in the Marshall et al. reference is shown or taught an application layer, a physical layer or an interconnect layer.

Secondly, nowhere is shown or taught a "reconfigurable" interconnect layer, much less a "reprogrammable" layer to provide a different switching function.

Note in Marshall et al. it is the purpose of the Marshall et al. system "core" to reconfigure the FPGAs, not the data pipes. These buses remain static and do not in and of themselves switch anything.

Note that Marshall et al. say that the FPGA's "customizable application core" is what does the reprogramming of their FPGAs. This is where the FPGAs are reconfigured; not by using a switchable interconnect layer, and especially not one coupled to a physical layer.

In short, what is uploaded to the space craft are

> "commands involving messages which reconfigure the basic signal-processing components utilized. What this means is that the instruction set for the FPGAs can be changed on the fly...so that the original or new hardware processing function is defined, thus to be able to reconfigure or create a new signal processor where one has (been) previously damaged or where the mission task has changed requiring different types of signal processing."

What is thus eminently clear is that Marshall et al. do not teach or suggest the claimed invention and in fact teach away from the claimed invention. They do this because Marshall et al. teach reprogramming "the core" of the FPGA, not any interconnect layer. In fact there are no reconfigurable or switchable interconnect layers mentioned in Marshall et al.

For these reasons it is Applicants' contention the claims are in condition for allowance. Allowance of the claims and issuance of the case is earnestly solicited.

Respectfully submitted,

Robert K. Tendler
Reg. No.: 24,581
65 Atlantic Avenue
Boston, MA 02110
Tel: (617) 723-7268

Date: April 22, 2009